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BUILT-IN SELF TEST FOR REGISTER FILE MEMORY COMPILER

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In modern telecommunication systems there are a lot of SoCs containing microprocessors, for which a Register File memory (RF) serving as an internal cache is one of the key components affecting the overall system performance [1]. The RF memory compiler is a special software consisting of the design library, scripts and other files, which contain the technology data necessary to generate RF instances [2]. Along with such requirements as area, speed and power consumption, there is a task for every single RF to pass functional testing as a standalone element of the chip. The Built-In Seft Test (BIST) is designed for on-chip testing purposes, as it is much easier to test an embedded RF/SRAM using a BIST than it is with an external high-cost equipment [3]. To allow for easy BIST integration, its data muxes were integrated into the memory circuitry so that the timing convergence is easier to achieve.

The designed RF memory compiler allows to generate a single RF instance with a number of words from 16 to 256 with a word step of 4 and a word length from 8 to 72 bit with a step of 1 bit. The total of 23040 different RF variants of instances can be generated. RF clock signal during compilation can be set in three ways: a single clock for two ports, two independent clocks for two ports, or two independent clocks with a conflict controller. The last option allows to delay write operation by storing the input word in the input port registers if read operation at the current address has already started – this helps to avoid loss of information.

When the BIST option is specified, its layout is generated, which includes the following main circuits: a test data sequence generator, a word address generator, comparators for comparing input data and reading data, and a control unit. The BIST configuration parameters are equal to the RF parameters, defining the length of the word being tested, the number of addresses and the length of the test sequence. At the same time, muxes of the write port, address signals, and write enable (**WEN**) and read enable (**REN**) signals are activated directly in the RF. As it is shown on the Fig. 1, this allows signals from the BIST circuitry to be connected to the RF inputs instead of using external signals for testing. The BIST output signals are: internal **BISTE** signal for switching the RF to the test mode, data and address signals, BIST read (**BREN**) and write (**BWEN**) commands. External signals at the output of the circuitry are: **BFAIL** – for read error and **BSTOP** – for end of

the testing, which are output to the input blocks (chip contact pads). There is an external BIST signal with the same name **BIST**, which begins the testing process.

In the test mode BIST runs the following sequence of six patterns for each of RF instances under the test [4]: (1) write solid "0" to port A; (2) read solid "0" from port B; (3) write solid "1" to port A; (4) read solid "1" from port B; (5) write checkerboard "0" to port A; (6) read checkerboard "0" from port B. Clocks signals are connected to both the RF and the BIST inputs. The total number of clock cycles for complete RF testing is: (**6xN + 2)**, where N is the number of RF words. To test the RF chips using BIST, a test structure was designed containing three types of RF instances of different sizes: (1) 84x24 bits with a single clock; (2) 134x39 bits, two clock signals for the write and read ports. (3) 256x72 bits, two clock signals for the write and read ports with the conflict controller.

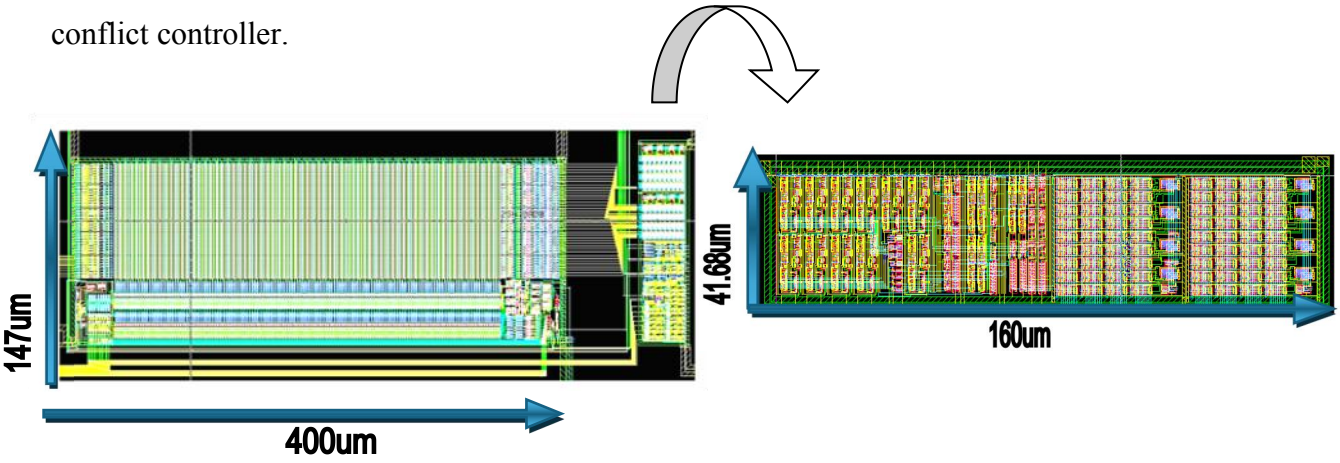

Fig 1. – Layout view of RF memory and BIST instance (134x39 bit configuration)

Conclusion

Area optimization achieved - the dimensions of a single BIST block are almost eight times smaller (6720µm2) than the dimensions of one the RF instance (58800µm2) of 134x39 bit configuration. If there were no build-in means to test the RF chip, it would have been necessary to have the following pad for the external signals: 8+8 for write and read port addresses; 39 + 39 for input and output data; 3 to control of mux of addresses and data, RF control units and test mode; In total there are 97 contact pads required that is an unacceptable amount. In addition, extra chip area is required in order to route 97 buses to the RF. The examined test structure was proved in silicon using both an external hardware tester equipment and the internal BIST. After having passed the sequence of 6 tests all three RF samples showed correct functioning when both methods applied.

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